REMARKS

An Office Action was mailed for the present application on April 12, 2006. A Response was filed, along with a petition for a two-month extension of time, on August 28, 2006. A Notice of Non-Compliant Amendment was mailed on September 12, 2006, due to claim 13 being inadvertently omitted from the Response. Therefore, this Supplemental Response is submitted to correct that error.

For the convenience of the Examiner, all remarks submitted in the Response of September 12, 2006, are presented herein in their entirety.

In the Office Action mailed on April 12, 2006, the Examiner noted that claims 1-13 are pending in the application, and the Examiner rejected all claims. The Examiner's rejections are traversed below, and reconsideration of all rejected claims is respectfully requested.

Claim Rejections Under 35 USC §102

In item 4 on pages 2-3 of the Office Action the Examiner rejected claims 1-12 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,044,451, issued to Slavenburg et al. (hereinafter referred to as "Slavenburg"). The Applicants respectfully traverse the Examiner's rejections of these claims.

Claim 1 of the present application recites "determining whether said basic instruction can be assigned to a logical instruction slot through checking a relationship between said classification of said functional slot and said logical instruction slot." In other words, the basic instruction is evaluated to determine whether it can be assigned to a logical instruction slot, which is not an actual instruction slot, before being assigned to an actual instruction slot. The Applicants respectfully submit that Slavenburg does not disclose at least this feature of claim 1.

The Examiner stated that Slavenburg determines whether said basic instruction can be assigned to a logical instruction slot through checking a relationship between said classification of said functional unit and said logical instruction slot. In support of this statement, the Examiner cited Lines 29-30 of Column 4 of Slavenburg, which states that "the issue slots all have some way of identifying which functional unit is to execute the operation." The Examiner cited this language of Slavenburg as disclosing steps to ensure validation of the issue slot, and further stated that "the mechanism Slavenburg implements to validate the contents of the issue slot is the imaginary slot Applicant calls 'the logical instruction slot'."

However, the Applicants respectfully submit that Slavenburg merely discloses routing the basic instructions to specific functional units which are identified in the instructions themselves. "[A]ll of the issue slots have a UNIT ID field, which identifies which functional unit the operation is destined for. For a machine of up to 8 functional units, this UNIT ID field need only be three bits wide" (Column 4, Lines 31-32). Therefore, each instruction has a specific code that defines the exact destination, i.e., the exact functional unit, to which the code is to be delivered. Hence, not only is no logical instruction slot disclosed, it is not even contemplated in the disclosure of Slavenburg, because there is no need for an evaluation of an instruction vis-à-vis a logical instruction slot when the instruction is provided with an exact road map to its actual destination instruction slot.

Further, while the Examiner stated that Slavenburg discloses "steps to ensure validation of the issue slot," the Applicants respectfully submit that no support can be found for this statement in the disclosure of Slavenburg. The language in Slavenburg cited by the Examiner, "the issue slots all have some way of identifying which functional unit is to execute the operation," merely shows that the issue slots read the UNIT ID fields in the instructions before sending the instructions to the specified functional unit. Even in an alternative embodiment mentioned in Slavenburg, in which the instruction implies the type of functional unit instead of a specific functional unit, no "steps to ensure validation of the issue slot" are undertaken. Rather, the instructions are merely entered into the issue slots before being routed to the applicable functional units. There is no validation of the issue slot, because the three operation slots of the VLIW instructions are merely delivered to the three available issue slots of the instruction issue register regardless of the operation type of the operation slots.

Even assuming, arguendo, that "steps to ensure validation of the issue slot" were discloses in Slavenburg, this would not disclose "determining whether said basic instruction can be assigned to a logical instruction slot through checking a relationship between said classification of said functional unit and said logical instruction slot," as recited in claim 1, because the steps would be taken by the actual issue slots of the instruction issue register after the instructions are delivered to the register ("Second, the issue slots all have some way of identifying which functional unit is to execute the operation", Column 4, Lines 29-20). It is apparent that if there were any determination of validation existing in Slavenburg, it would be in relation to the actual instruction slot, and by the actual instruction slot, rather than a logical instruction slot.

Therefore, the Applicants respectfully submit that Slavenburg does not disclose or suggest "determining whether said basic instruction can be assigned to a logical instruction slot through checking a relationship between said classification of said functional unit and said logical instruction slot."

Claim 1 also recites the feature of "assigning, to an instruction slot, said basic instruction determined to be assignable to said logical instruction slot." The Applicants respectfully submit that Slavenburg also does not disclose at least this feature of claim 1.

As explained above, there is no logical instruction slot disclosed, suggested, or contemplated by Slavenburg. Therefore, it would not be possible that Slavenburg could contemplate assigning a basic instruction to an instruction slot based on a determination that the instruction is assignable to a logical instruction slot.

Further, even assuming, arguendo that any determination whatsoever was being conducted with a logical instruction slot, this would have no bearing in Slavenburg in regard to which basic instruction is assigned to which instruction slot of the instruction issue register. Slavenburg discloses a method in which the number of operations of the VLIW instructions are all matched to the number instruction slots in the instruction issue register. In other words, if there are three instruction slots in the register, there will be three operation instructions in the VLIW. "In the VLIW CPU of FIG. 3, in each clock cycle, a three operation instruction is issued from the IIR" (Column 4, Lines 41-42). Because all of these VLIW instructions are in the three operation format, as clearly illustrated in Figure 4 of Slavenburg, and the instruction issue register has three issue slots, as clearly illustrated in Figure 4 of Slavenburg, the three operations (instructions) are sent to the three issue slots in a one-to-one manner. Therefore, the first, second, and third operations of the VLIW are respectively sent to the first, second, and third issue slots of the instruction issue register. Thus, the issue slot to which the instructions are sent depends solely on which slot the instruction occupies in the VLIW. This is in direct contrast to claim 1 of the present application, which recites "assigning, to an instruction slot, said basic instruction determined to be assignable to said logical instruction slot." No determination is made in Slavenburg regarding which instruction goes to which instruction slot (much less a logical instruction slot), because it is solely dependent upon where the instruction is stored in the VLIW.

Therefore, Slavenburg does not disclose at least the features of claim 1 discussed above. Accordingly, Slavenburg does not disclose every element of the Applicants' claim 1. In order for a reference to anticipate a claim, the reference must teach each and every element of

the claim (MPEP §2131). Therefore, since Slavenburg does not disclose the features recited in independent claim 1, as stated above, it is respectfully submitted that claim 1 patentably distinguishes over Slavenburg, and withdrawal of the §102(e) rejection is earnestly and respectfully solicited.

Claims 2-8 depend from claim 1 and include all of the features of that claim plus additional features which are not disclosed or suggested by Slavenburg. Therefore, it is respectfully submitted that claims 2-8 also patentably distinguish over Slavenburg.

Claim 9 of the present application recites similar features to those discussed in regard to claim 1. Further, claims 10-12 depend from claim 9 and include all of the features of that claim plus additional features which are not disclosed or suggested by Slavenburg. Therfore, it is respectfully submitted that claims 9-12 also patentably distinguish over Slavenburg.

In item 5 on page 3 of the Office Action the Examiner rejected claim 13 under 35 U.S.C. §102(a) as being anticipated by Miyake et al. (EP 1,089,168, hereinafter referred to as "Miyake"). The Applicants respectfully traverse the Examiner's rejections of these claims.

Claim 13 of the present application recites "arranging, via computer, variable-length instructions to be executed in an order in a logical instruction slot; and verifying an arrangement of the variable-length instructions." The Applicants respectfully submit that these features are not disclosed by Miyake.

The Examiner stated that Miyake discloses arranging variable-length instructions to be executed in an order in a logical instruction slot, and verifying an arrangement of the variable-length instructions, citing paragraphs [0067]-[0069] and Figure 9 of Miyake. However, the Applicants respectfully submit that Miyake discloses rearranging instruction word formats, through a conversion unit, into word formats which correspond to the instruction execution units. The Applicants respectfully submit that this does not anticipate the logical instruction slot recited in claim 13 of the present application, nor the verification of the arrangement produced in the logical instruction slot. Thus, the Applicants respectfully submit that claim 13 of the present application patentably distinguishes over Miyake.

Summary

There being no further outstanding objections or rejections, it is respectfully submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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